Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A semiconductor device comprising:

a substrate;

a plurality of inter-level dielectric (ILD) layers each having a low dielectric constant (k);

at least one support structure disposed in ~~in~~ each of the ILD layers at locations overlying each other so that support structures overly each other in the plurality of layers to mitigate damage of the semiconductor device caused by stresses to the ILD layers;

at least one additional ILD layer having a dielectric constant which is higher than the low-k ILD layers overlying the low-k inter-level dielectric layers; and

a contact layer overlying the at least one additional ILD layer and the support structures, wherein the at least one additional ILD layer isolates the contact layer from the support structures.

2. (Previously presented) The semiconductor device of claim 1, wherein at least one ILD layer has an ultra low dielectric constant (k).

3. (Original) The semiconductor device of claim 1, wherein the at least one support structure is one of a trench and via formed from a support material.

4. (Original) The semiconductor device of claim 3, wherein the support material comprises at least one of aluminum, aluminum alloy, copper, copper alloy, tungsten, or tungsten alloy.

5. (Original) The semiconductor device of claim 1, wherein the support structure mitigates damage of the ILD layer due to forces applied onto the ILD layer during one of a subsequent processing and packaging of the semiconductor device.

6. (Cancelled)

7. (Previously presented) The semiconductor device of claim 1, wherein the support structures are located underneath the source of the stress to mitigate damage to the semiconductor device.

8. (Original) The semiconductor device of claim 7, the source of the stress being a bond pad location.

9. (Cancelled)

10. (Previously presented) The semiconductor device of claim 1, the support column ending at the at least one additional ILD layer

11. (Cancelled)

12. (Currently amended) A semiconductor device comprising:

a substrate;

a plurality of inter-level dielectric (ILD) layers each having a low dielectric constant (k);

at least one support structure disposed in ~~in~~ each of the ILD layers at locations overlying each other so that support structures overly each other in the plurality of layers to mitigate damage of the semiconductor device caused by stresses to the ILD layers;

at least one additional ILD layer having a dielectric constant which is higher than the low-k ILD layers overlying the low-k inter-level dielectric layers; and

a contact layer overlying the at least one additional ILD layer and the support structures, wherein the at least one additional ILD layer isolates the contact layer from the support structures;

wherein a plurality of support structures are disposed in at least one of the low-k dielectric layers in an n x m matrix configuration, where n and m are integers greater than one; and

wherein the plurality of support structures are disposed at a location below a bond pad disposed on the semiconductor device .

13. (Original) The semiconductor device of claim 12, wherein a plurality of support structures are disposed in the at least one low-k dielectric layer at a plurality of locations spaced equidistant apart from each other across substantially the entire layer.

14-23. (Canceled)

24. (Currently amended) A semiconductor device comprising:

a substrate;

a plurality of inter-level dielectric (ILD) layers each having a low dielectric constant (k);

at least one support structure disposed in ~~in~~ each of the ILD layers at locations overlying each other so that support structures overly each other in the plurality of layers to mitigate damage of the semiconductor device caused by stresses to the ILD layers;

at least one additional ILD layer having a dielectric constant which is higher than the low-k ILD layers overlying the low-k inter-level dielectric layers; and

a bond pad overlying the at least one additional ILD layer and the support structures.